Driving and Biasing PSPL Edge Compressor Components

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INTRODUCTION

Picosecond Pulse Labs (PSPL) offers a family of Edge Compressors that can generate electronic signals with edge transition times as short as 4 picoseconds at amplitudes as great as 10 volts. Figure 1 shows the effect of a properly biased 7003P Edge Compressor on a 7 volt step with a 35 ps risetime. This device, with its large output voltage, extremely fast risetime, and broad bandwidth, will provide outstanding performance improvements in the implementation of ultra-fast samplers, comb frequency generators, harmonic multipliers, impulse generators, TDR and TDT sources, UWB transmitters, and risetime calibration standards. This Application Note will introduce the characteristics and performance of edge compressors, paying particular attention to the bias and termination required to optimize results.
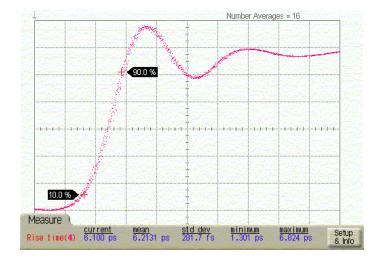

Figure 1: 7003P Compression Example
Output is 5.8 V, < 4 ps risetime. Measurement made using PSPL 100 GHz sampler (risetime = 3.5 ps) and a PSPL Model 5510-V-20 dB attenuator (risetime < 5 ps). Total measurement system risetime is 5.7 ps. Input is a 7 Vptp, 35 ps risetime signal. Scales are 1 V/div and 5 ps/div.

EDGE COMPRESSOR CHARACTERISTICS

The Model 7000 edge compressors are implemented as coaxial components measuring less than 1.5"x0.5"x0.25" and equipped with an input jack and an output plug. They use Non-Linear Transmission Line (NLTL) technology and may be modeled as a synthetic transmission line structure with series inductance and shunt voltage-variable capacitance provided by varactor diodes (Figure 2). They are available in two polarities: grounded anode for positive drive signals (7001P, 7002P, and 7003P) and grounded cathode for negative drive signals (7001N, 7002N, and 7003N). The three versions of each polarity are further characterized by the total amount of edge compression available and by the limiting transition time at the output. Please refer to the specification sheet available on our Web site for details.
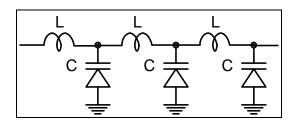

Figure 2: Simple Schematic Diagram

The positive polarity edge compressors will be described in this Application Note. The three P versions are designed for an input operating range of –0.7 volts (the diode forward bias voltage) to +10 volts (the diode breakdown voltage). Typical values of compression and limiting risetime for these models are shown in Table 1.

Model	Compression (ps)	Limiting Risetime (ps)
7001P	40	20
7002P	25	4
7003P	65	4

Table 1: Typical Characteristics of Edge Compressor Models

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Risetime compression is a direct consequence of the voltage dependent line capacitance. The varactor capacitance is greatest when the diode is forward biased and decreases as the diode is reversed biased. The values of L and C in the transmission line determine the propagation delay and the characteristic impedance. Table 2 shows the typical range of these parameters for the 7003P. The small signal group delay through the device is greatest with slight forward bias and least at reverse voltages near breakdown (Figure 3). For a positive pulse input waveform transitioning from – 0.7 volts to + 6 volts, the low voltage components will be delayed more than the high voltage components, effectively reducing the risetime of the output leading edge. The fall time of the trailing edge will be increased (Figure 4). The output transition time limit is reached when the edge compression due to the varactors is cancelled by the dispersion due to the periodicity of the synthetic transmission line. For the 7003P, an input signal with a risetime of less than 65 ps is required to produce an output risetime of 4 ps.

Bias Voltage	Insertion Delay	Impedance
+7.0 V	247 ps	49 Ohms
0.0 V	285 ps	37 Ohms
- 0.5 V	315 ps	32 Ohms

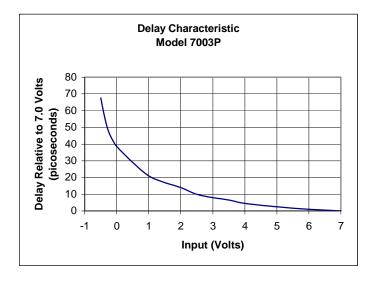**Table 2: 7003P Voltage Dependant Insertion Delay and Characteristic Impedance**

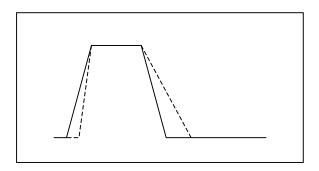**Figure 3: Delay of 7003P Edge Compressor versus Input Voltage (relative to +7 volts)**

Figure 4: The Positive Polarity Edge Compressor Reduces the Risetime and Increases the Fall Time.
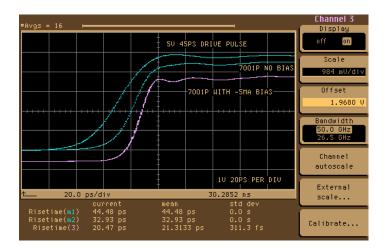
TERMINATIONS

With proper termination, the edge compressors can be driven to the 10 volt maximum rating determined by the avalanche breakdown of the varactor diodes. A 50 ohm DC termination will deliver the best device performance. Exercise extreme caution when attempting to drive something other than a 50 ohm load.

- A load should always be connected to the edge compressor before drive power is applied.

- Transmission line reflections can increase the output beyond the edge compressor breakdown voltage.

- Reflections due to an open-circuit load, like an antenna, will potentially double the signal at the edge compressor output.

- AC-coupled loads driven at low repetition rates can subject the edge compressor to twice the generator output voltage. The input voltage should be limited to 5 volts for this case.

- A DC short circuit (such as a transformer) connected to the output of the edge compressor can defeat attempts to forward bias the diodes.

BIASING

In general, edge compressors give the best performance when the diodes are forward biased. A significant part of the total group delay change occurs in the forward bias region as shown in Figure 3. Figure 5 shows the increased compression obtained when the input signal baseline is biased to –0.5 volts instead of zero volts.

**Figure 5: Edge Compression Using a
PSPL Model 7001P**

Traces show the +5 volt 45 ps risetime input drive pulse, the 7001P output with no bias, and the 7001P output with -5 mA of bias current.
Measured with Agilent 54750A, 50 GHz, 8.6 ps oscilloscope and PSPL 5510-V-20 dB, < 5 ps attenuator. Scales are 1 V/div and 20 ps/div.

**Figure 6: Pulse Edge Compression with Cascaded
PSPL Models 7001P and 7002P**

Traces show the +5 volt, 45 ps risetime input drive pulse, the 7001P output, and the 7002P output. Forward bias current was provided through a PSPL 5545 bias tee on the output of the 45 ps drive pulse generator. Measured with Agilent 54750A, 50 GHz, 8.6 ps oscilloscope and PSPL 5510-V-20 dB, < 5 ps attenuator. Scales are 1 V/div and 20 ps/div.

A DC return path is required for proper control of the diode forward bias current. The following techniques are useful:

- A bias tee (like the PSPL Model 5545) can be placed between the source and the edge compressor so the diode forward bias current can be controlled and monitored. This is especially effective for low duty-cycle waveforms.
- A 1 dB attenuator can be used as a DC return between the edge compressor and an AC-coupled source.

CASCADING EDGE COMPRESSORS

PSPL's edge compressors can be cascaded to increase the risetime compression. Figure 6 shows the result of cascading a 7001P with a 7002P. The 45 ps input risetime was first compressed to 20 ps by the 7001P and then further compressed to less than 12 ps by the 7002P. It should be noted that the actual 7002P output risetime is considerably faster than shown in Figure 6. The Agilent 50 GHz oscilloscope and the 20 dB attenuator limit the risetime measurement.

DRIVE WAVEFORMS

PSPL edge compressors can be driven with a variety of waveforms, including low duty cycle pulses, sine waves, and logic signals. The key points to follow when designing the drive circuits for maximum edge compression are:

- Use signal amplitudes of about 5 to 6 volts. Voltages at this level are far less likely to cause reverse voltage breakdown problems, and there is little group delay change for voltages between 6 and 10 volts.
- Use forward bias current, but observe the maximum ratings.
- Use a drive signal with a risetime less than the sum of the rated compression time and the limiting output transition time of the device.
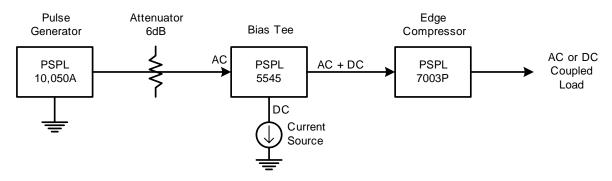- Always provide a DC return path for diode current.

Figure 7: Pulse Drive with Bias Tee

Low Duty Cycle Pulse Drive

Pulse generators such as the PSPL models 4015C, 4050B, 10,050A, 10,060A, and 10,070A are suitable drivers for the PSPL 7000 series edge compressors. For example, the results shown in Figure 5 and Figure 6 were produced using a PSPL model 10,050A, 45 ps risetime pulse generator. As shown by Figure 7 the 10,050A +10V output pulse was attenuated by a PSPL model 5510, 6 dB SMA attenuator, and then coupled through a PSPL Model 5545 bias tee to the edge compressor. The bias tee was used to inject a forward DC bias current of about 5 mA to enhance the edge compression.

Sinusoidal Drive

Sinusoidal drive is one of the simplest methods of exciting the PSPL edge compressors. However, it only works well at frequencies above about 4 GHz.

Best results are achieved by using about +20 dBm of sine wave drive power (6.3 Vptp) into the edge compressor. The 7003P must be biased so that the negative portion of the sine wave drives the diodes slightly into forward bias.

Figure 8 shows an effective way of setting the bias. The sine wave source is coupled through the AC port of a bias tee to the edge compressor, and the bias is established through the DC port. This provides a means to monitor as well as control the magnitude of the bias current to optimize the edge compression. The diode current should be set to about 5 mA. When set correctly, the positive going edge of the sine wave will be compressed and the trailing edge will be expanded, resulting in a sawtooth waveform. This method can be used for either an AC-coupled load or a DC-coupled load.
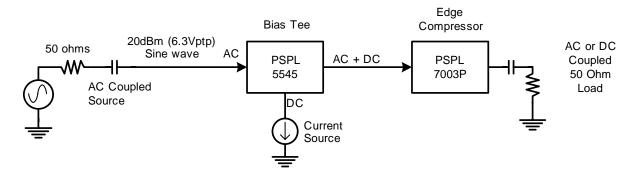

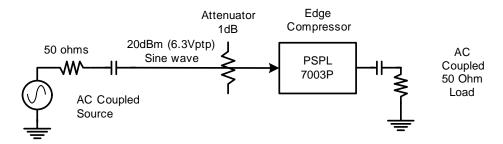**Figure 8: Sine Wave Drive with Bias Tee**

Figure 9: Sine Wave Drive without Bias Tee

Figure 9 shows a second bias arrangement that is usable only for an AC-coupled load. An SMA 1 dB attenuator is connected between the AC-coupled sine wave input and the edge compressor. The DC resistance to ground of the 1 dB attenuator (approximately 435 ohms) provides the necessary DC return path for the rectified diode current and provides the proper bias current. A DC–coupled 50 ohm load will result in too much diode bias current. The resulting sawtooth waveform is shown in Figure 10.

Logic-Level Drive

Conventional logic families (TTL, CMOS, ECL, and CML) do not provide large enough voltage levels or fast enough transitions to directly drive PSPL edge compressors to their best performance. Figure 11 shows how a PSPL Model 5865 Amplifier/Driver can be used to amplify logic signals to 8 Vptp with a rise time less than 60 ps. This will still require an input to the 5865 of about 1 Vptp with a rise time less than 150 ps.
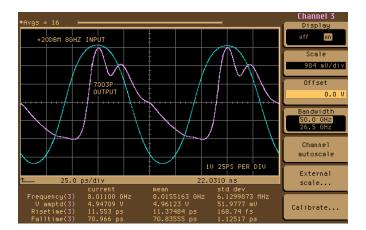

Figure 10: Sine Wave Driven Edge Compressor
The drive signal was +20 dBm, 8 GHz sine wave.
A PSPL Model 5510,1 dB SMA attenuator was used on the input to provide a DC return path.
The edge compressor was a PSPL model 7003P.
The output was AC-coupled through a PSPL model 5509 DC Block. Measured with Agilent 54750A, 50 GHz, 8.6 ps oscilloscope and PSPL 5510-V-20 dB, < 5 ps attenuator. Scales are 1 V/div and 25 ps/div.
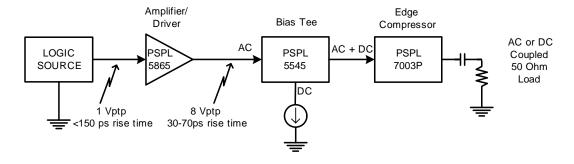

Figure 11: Using a Model 5865 Amplifier/Driver to Boost Logic Signal Levels

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