

Generation of 10 ps Risetime, Differential, Test Signals

James R. Andrews, Ph.D, IEEE Fellow PSPL Founder & former President (retired)



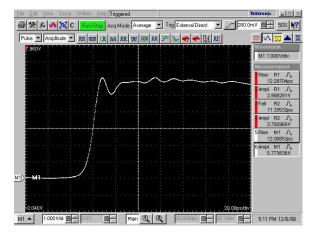


Fig. 1 PSPL model 4022 - Differential Pulse Generator 1 V/div & 20 ps/div

The Picosecond Pulse Labs (PSPL) model 4022 pulse generator can be used to supply < 10 ps risetime differential test signals to test many different ultra-high-speed logic families. The PSPL model 4022 is capable of generating differential Step Function test pulses with amplitudes up to approximately 5 Volts. With the addition of PSPL model 5206 IFNs, 1.5 Volt, 17 ps differential Impulse test pulses can also be generated. To create specific logic level signals (such as PECL), the pulse amplitudes need to be attenuated, and the 0 V baselines need to be offset. The amplitudes can be set by adding fixed attenuators. The PSPL model 5510-V-XdB is recommended. The baseline offset is accomplished by adding a pair of bias tees on the attenuated positive and negative pulse outputs. The PSPL model 5542 with 2.4mm connectors is recommended.

The PSPL model 4022 was originally designed to be used as a risetime enhancer for use with Agilent and Tektronix TDRs (<u>Time Domain Reflectometers</u>). Although the 4022 is labeled as a TDR/TDT Enhancement Module, it does not need to be used for these applications, nor does it require the user to purchase an expensive TDR.

The Agilent and Tektronix TDRs typically produced 200 mV TDR step pulses with risetimes of the order of 25 to 35 ps at pulse repetition rates of 100-200 kHz. The 4022 was designed to be triggered by these slow rise TDR pulses and output much faster (< 10ps), 200 mV TDR pulses or 2.5 V pulses for TDT (Time Domain Transmission) testing. The type (TDR or TDT) and polarity (Pos or Neg) of the pulse is determined by which Pulse Head is used with the 4022. The 4022 was designed to automatically sense which pulse head is attached and drive it appropriately. When triggered, the 4022 produces fixed duration pulses of typically 40 ns.

TRIGGERING REQUIREMENTS: The PSPL model 4022 does not include its own internal rep. rate clock. It must be triggered externally. However, the 4022 does NOT need to be triggered by a dedicated TDR pulse. Thus the user is not obligated to purchase an expensive TDR module from Agilent, Tektronix, or LeCroy to simply trigger the 4022. Most any other pulse generator can be used to trigger the 4022. The 4022's Trigger Input is AC coupled and terminated in 50 Ohms. The 4022 triggers on a positive-going slope. The trigger pulse amplitude must be > 50 mV and < 1 V. The damage threshold is 1 Volt. The most reliable triggering is achieved at 400-500 mV amplitude. The trigger pulse duration (width) must be > 50 ns. Narrower pulses will create false triggering. The

trigger rep. rate should be kept below 1 MHz. Higher rep. rates will cause severe baseline shifting and waveform distortion. For optimum, very low timing jitter performance, the trigger pulse risetime should be < 500 ps. With a Tektronix 70 GHz, 5 ps, sampling oscilloscope (model TDS-8000 main frame and 80E06 sampling head), the overall system (4022 + o'scope) jitter is typically 1 ps rms. If the trigger risetime is slower than 500 ps, the jitter will degrade. With a 3 ns trigger risetime, the jitter is 2 ps rms.

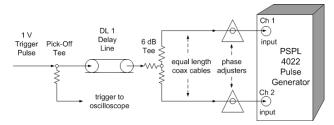


Fig. 2 Differential Triggering Set-Up

DIFFERENTIAL TRIGGERING: The 4022 consists of two identical 4020 pulse modules housed in a single cabinet. Thus, there are two independent trigger inputs and two independent remote pulse head driver outputs. For generating differential pulses, both of the 4022's trigger inputs need to be driven. See Figure 2 for the recommended arrangement. A 1 Volt input trigger pulse is split into two identical, 500 mV pulses by the 6dB Tee, Power Divider. The PSPL model 5331 is recommended for this application. Identical lengths of short, SMA cable are then used to connect the 6dB tee outputs to the 4022 trigger inputs. These are located on the 4022's rear panel. While both channels of the 4022 are rather closely matched in terms of throughput delay, they are not absolutely identical. Thus PSPL recommends that the user also insert a pair of SMA phase adjusters on the trigger inputs. (PSPL uses Coaxicom model 3993-1.) To achieve the ultimate differential performance, the outputs from the positive and negative pulse heads should be phase matched to < 1 ps. This is easily accomplished using the Coaxicom phase adjusters.

To achieve the ultimate, low jitter performance, PSPL recommends that the measurement oscilloscope not be triggered by the trigger output from the pulse generator used to trigger the 4022. Any jitter present between that generator's trigger and main pulse outputs will immediately translate into added jitter on the 4022's pulses. The lowest jitter triggering is achieved by using a pick-off tee for

the oscilloscope's trigger and then inserting a fixed length of good quality, coax cable between the pick-off tee and the 6dB Tee. See Figure 2. A suitable pick-off tee is the PSPL model 5370. The throughput delay of the 4022, including its pulse heads and interconnecting cables, is typically 5.5 ns. Use only enough additional delay cable, DL 1 in Figure 2, to provide the required pre-trigger delay for the oscilloscope. For example, the 70 GHz, 5ps, Tektronix oscilloscope used for the examples here requires 19 ns pre-trigger delay.

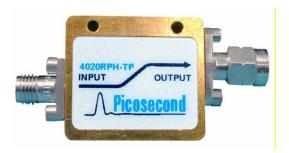


Fig. 3 4020RPH-T pulse head

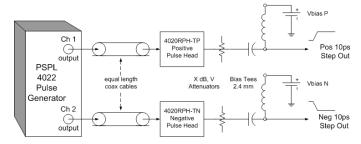


Fig. 4 Differential Step Generator Set-Up

STEP GENERATOR: Connect the Pulse Heads, Attenuators, and Bias Tees as shown in Figure 4. Pay particular care to the types of connectors used. The 4022 drive pulse outputs and the yellow, pulse head cables use SMA connectors. The drive pulse input to the 4020RPH pulse heads also uses an SMA connector. The pulse head output connector is a 2.4 mm. The 5542 bias tee connectors are also 2.4 mm, while the attenuator uses 1.85 mm connectors. 1.85 mm and 2.4 mm are interchangeable, but will not mate with SMA, 3.5 mm nor 2.9 mm.

While the 4020RPH TDT, 2.5 V pulse heads were used for this note, the 4020RPH TDR pulse heads could also be used. However, the output pulse amplitudes will be much lower (200 mV).



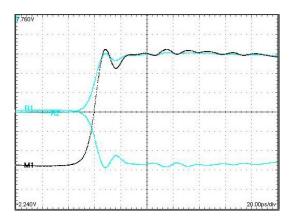


Fig. 5 Differential Step Waveforms. No offset bias applied. 1 V/div & 20ps/div

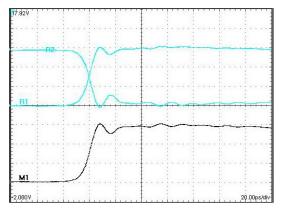


Fig. 6 Differential Step Waveforms with offset bias voltages applied to bias tees.

V+ & V- at 1 V/div (top), V_{diff} at 2 V/div (bottom trace) & 20ps/div

Figures 5 and 6 show the resultant step waveforms. The cyan traces are the V+ and V- pulse outputs. The black trace is the differential voltage waveform $(V_{diff} = V + - V -)$. Figure 5 is with no offset voltage applied to the bias tees. For proper testing of logic devices, the proper offset voltages need to be applied to the bias tees to position the positive and negative polarity waveforms as shown in Figure 6. No attenuators were used for Figures 5 and 6. Typical max. amplitude values are 2.5 V for V+ and V- and 5 V for V_{diff}. The V+ risetime, V- falltime, and V_{diff} risetime all are < 10ps. It should be noted that it is extremely important to have the positive and negative waveforms precisely phase matched at the 50% crossing level. Any phase offset will translate immediately into an equal slowing of the differential signal's risetime. This phase adjustment is easily performed using the Coaxicom phase adjusters (see Figure 2).

IMPULSE GENERATOR: An ultra-narrow, Impulse generator can be easily configured by adding a PSPL model 5206 IFN (Impulse Forming Network) between the Pulse Head and the attenuator. See Figure 7. Typical max. amplitude values are > 0.5 V for V+ and V- and > 1 V for V_{diff} . The V+, V-, and V_{diff} durations all are < 17ps. As with the step, it is also vitally important to precisely phase match the positive and negative impulses. This is done by using the trigger input phase adjusters to align the peak and valley of the V+ and V- waveforms as shown in Figure 9.

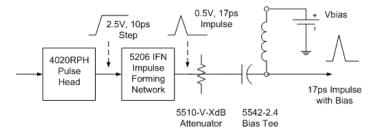


Fig. 7 Impulse Generator Set-Up



Fig. 8 PSPL model 5206 IFN

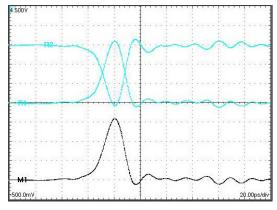


Fig. 9 Impulse Generator Outputs V+ & V- at 250mV/div (top), V_{diff} at 500mV/div (bottom) & 20ps/div